**ECE3205 – Lab 2**

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**Objective:**

The objective of this lab is to practice writing a VHDL design without using a dedicated IDE, such as Xilinx.

**Equipment, Procedure, and Data:**

Equipment needed:  
 - Computer with Xilinx (or other VHDL libraries) and Questa software  
 - Provided code to copy into the software

Procedure:

1. Create a working directory via command line
2. Create new files for each of the specified designs
3. Copy the code from the textbook for each of the designs
4. Compile the design using the vcom command in command line
5. Use the vsim command to start the simulation software (Questa)
6. Test the design in simulation

**Analysis and Discussion:**

The design that had all components of the full adder described in a single file would not compile, returning an error that half\_adder and or\_2 were unknown entities. This problem was not resolved.

The remaining three independent designs of full\_adder, half\_adder, and or\_2 had minor syntax and semantic errors that were resolve. They then simulated successfully

**Conclusions:**

The goal of this lab was to become familiarized with writing functional VHDL without a dedicated IDE. The bulk of time spent on the lab was spent troubleshooting compiler errors that mostly arose from syntax and semantic errors, some of which I was not able to resolve. Learning and gaining familiarity with writing a design without needing to use ModelSim directly has given me more confidence in my understanding of VHDL.